REMARKS/ARGUMENTS

The above-identified patent application has been amended and reconsideration and re-examination are hereby requested.

Portions of the Summary Section and claim 2, 3 and 4 have been amended to correct typographical or inadvertent errors.

Before discussing the claims and how they distinguish over the cited art, as pointed out in the patent application on page 10, lines 4-9:

> When data is sent over the channel it is split across the 2 serial links that make up that channel ***so that half goes on the high link (for, as noted above, the most significant bits)*** and ***half goes on the low link (for, as noted above, the least significant bits).*** Unlike data, which can have different values on the high and low links (but both links must be sending data), identical semaphores must occur on both links at the same time to make sure that the links frames are properly aligned. (emphasis added)

Applicant automatically resets the serializer deserializer if there is a misalignment mismatches between the two links.

Referring to Mayweather et al. US 2002/0147947, it is first noted that Mayweather et al, is determining BER. Mayweather is not resetting the serializer-deserializer if there art misalignment mismatches between the two links. As stated in paragraphs [0014-0017] of Mayweather et al."

> [0014] In FIG. 1, the communications network 10 is shown transmitting a serial data stream to an input portion of the node 5 referred to as an 8B/10B layer 12. This 8B/10B format is convenient since error indications are available from the SERDES device, where error indications are provided independently of packet CRC's. However, the particular data format used by network 10 is not significant for carrying out the invention.
> [0015] In an 8B/10B format, ***a transmitting node converts an original 8 bit word of parallel bits into a serial word of 10 bits. There are two different 10 bit words that correspond to an original 8 bit word. One of the 10 bit words has a positive disparity, and the other 10 bit word has a negative disparity.*** Disparity refers to the balance of 1's and 0's in the transmitted data. The disparity of the 10 bit word is chosen in accordance with the 8B/10B standard

> to provide a neutral disparity over successive words. The 10 bit words are also devised so there is a maximum number of possible consecutive 1's and 0's that may be transmitted. A large number of sequential logical 1's creates baseline wander, a shift in the long-term average voltage level used by the receiver as a threshold to differentiate between 1's and 0's. By utilizing a 10-bit word with a balanced number of 1's and 0's, the baseline wander is greatly reduced. (emphasis added)
> [0016] Additionally, in certain systems, such as in SONET systems where the various nodes are synchronized with one another, transitions between 1's and 0's are used to synchronize clocks. More generally, systems which utilize clock and data recovery circuits to recover clock use transitions between 1's and 0's. The 8B/10B format ensures sufficient transitions to keep the clocks synchronized.
> [0017] Such an 8B/10B coding scheme is well known and commonly used in Gigabit Ethernet. Such encoding is described in detail in the book, "Gigabit Ethernet" by Rich Seifert, 1st ed., Addison Wesley Longmon, Inc., 1988, incorporated herein by reference. The 8B/10B standard is further described by Peter A Franaszek and Albert X. Widmer in U. S. Pat. No. 4,486,739, entitled "Byte Oriented DC-Balanced (0,4) 8B/10B Partitioned Block Transmission Code," assigned to IBM and incorporated by reference. One commercially available device for performing 8B/10B conversion is the model VSC7216UC-01 parallel-to-serial and serial-to-parallel transceiver chip by Vitesse Semiconductor Corporation, Camarillo, Calif. The VSC7216UC-01 data sheet is incorporated by reference. Such a chip is also referred to as a serializer-deserializer or SERDES.

Applicant fails to see described in Mayweather et al. a system wherein data is sent over the channel it is split across the 2 serial links that make up that channel ***so that half goes on the high link (for, as noted above, the most significant bits)*** and ***half goes on the low link (for, as noted above, the least significant bits).***

Another feature in Applicant's invention is noted. i.e., the reset is for the serializer-deserializer, as distinguished from the counter.

The Examiner points out that paragraph [0029] resets the serializer-deserializer; however such paragraph points out that ***the counter*** is reset not the serializer deserializer:

> [0029] A programmable count mask 24 receives the count from counter 22. Upon detecting a predetermined count from counter 22, the count mask 24 interrupts a CPU 25, used by the node for various functions, which

> then calculates the BER for the system. One skilled in the art would understand the simple software used by the CPU to calculate the BER. In one embodiment, the programmable count mask 24 detects when the counter 22 has reached the count of 250 prior to initiating the CPU interrupt. Using the Tchbeychev inequality, it has been shown that 250 errors are required to guarantee that greater than 99% of the time the BER measurement will differ by 10% or less from the actual BER. The fixed error threshold to trigger the calculation of the BER may be greater than or less than 250, such as between 100-1000, and preferably between 200-400. If the error threshold is too high, it will be difficult to count the time between BER measurements. If the error threshold is too low, the accuracy of the BER suffers. ***The error counter 22 is reset after the CPU reads the data.*** (emphasized)

Referring now to the claims:

Claim 1 points out that the system includes a transmitter board for transmitting a copy of signals produced in such system, the copy of such signals comprises serial data in a **low byte** serial link and in a **high byte** serial link, the signals include special characters interspersed in a pattern with the data in the low and high byte serial links. As noted above, such is not described in Mayweather et al.

Claim 2 points out that the logic maintains a count of the number of mismatches, such system providing the **reset signal to the serializer-deserializer** when a predetermined plurality of mismatches has been indicated. As noted above, such is not described in Mayweather et al.

Claim 3 points out that in the system the data is in a series a low byte serial link and a high byte serial link, such signals including with the data and special characters interspersed in a pattern with the data in the low byte serial link and interspersed with the data in such high byte serial link. As noted above, such is not described in Mayweather et al.

Claim 4 points out that such data in the series having ***lower significant bytes*** thereof in a low byte serial link and ***having more significant bytes thereof*** in a high byte serial link, such signals including with the data, special characters interspersed in a pattern with the bytes of each of the data in such low byte serial link and interspersed with the bytes of each of the data in such high byte link serial data. As noted above, such is not described in Mayweather et al.

Claim 5 points out that the copy of the memory board-to-director board portion has a high byte serial link and a low byte serial link and the copy of the memory board-to-director board portion having a high byte serial link and a low byte serial link. As noted above, such is not described in Mayweather et al.

Claim 9 further limits claim 8 by pointing out that

> each one of the adapter boards has a connector with a linear array of N pins, such pins being arranged in sets of four pins, each set of four pins for the copy of signals from the director board-to-memory board portion of each one of such primary channels passing signals and the copy of signals from the a memory board-to-director board portion of each one of such primary channels passing signals to provide N/4 redundant channels, where N is an integer greater than one; and
>
> each one of the analyzer boards has a connector with a linear array of M pins adapted for connecting to the connector of a corresponding one of the adapter board connectors,, where M =N/2, such analyzer board pins being arranged in sets of four pins, each set of four pins providing a receiving channel, such adapter board pins thereby providing M/4 receiving channels, each one of the M/4 receiving channels being adapted for connection to a corresponding one of the N/4 redundant channels thereby providing connections to N/2 redundant channels and N/2 unconnected redundant channels, one of the M/4 receiving channels being connected one of the redundant channels disposed adjacent to one of the unconnected redundant channels.

Applicant fails to see anything in Mayweather et al., or the prior art that suggests such an arrangement.

In the event a petition for extension of time is required by this paper and not otherwise provided, such petition is hereby made and authorization is provided herewith to charge deposit account No. 05-0889 for the cost of such extension.

In the event any additional fee is required, please charge such amount to Patent and Trademark Office Deposit Account No. 05-0889.

Respectfully submitted,

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Date

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